CLAIMS

What is claimed is:

1. A method for performing a delayed transaction, comprising:

receiving a read request from a PCI (Peripheral Component Interconnect) agent coupled to a PCI bridge;

allocating a pre-fetch buffer for the delayed transaction;

setting a buffer fill watermark for the pre-fetch buffer;

transferring data into the pre-fetch buffer while monitoring a fill level of the pre-fetch buffer; and

enabling data to be transferred from the pre-fetch buffer to the PCI agent once the fill level of the pre-fetch buffer meets or exceeds the buffer fill watermark.

2. The method of claim 1, further comprising programming a configuration register on the PCI bridge to set the buffer fill watermark.

3. The method of claim 1, further comprising determining a buffer fill watermark value by observing data transfer rates of the PCI agent when different watermarks are used.

4. The method of claim 3, further comprising dynamically setting the buffer fill watermark value.

5. The method of claim 1, further comprising:

(a) receiving a first read request to transfer data from system memory to the PCI agent, the first read request referencing an initial starting address at which the data is located;

(b) setting the buffer fill watermark to an initial value;

(c) receiving a current portion of the data at the PCI bridge;

(d) transferring at least part of the current portion of the data into the pre-fetch buffer while monitoring a fill level of the pre-fetch buffer;

(e) connecting the PCI agent to the PCI bridge in response to determining the fill level of the pre-fetch buffer meets or exceeds the buffer fill watermark;

(f) transferring data from the pre-fetch buffer to the PCI agent until the pre-fetch buffer is emptied or the PCI agent disconnects;

(g) receiving one or more subsequent read requests from the PCI agent, each subsequent read request having a starting address corresponding to a remaining portion of the data that has yet to be received by the PCI agent;

(h) repeating operations (c) – (g) until the data transaction is completed.

6. The method of claim 5, wherein the PCI agent comprises a multi-channel PCI device, and a respective set of operations (a)-(j) is performed for each channel to perform a plurality of concurrent delayed transactions.

7. The method of claim 6, wherein the multi-channel PCI device comprises a dual-channel mass storage device controller.

8. A method comprising:

receiving first and second data transfer requests from a multi-channel PCI (Peripheral Component Interconnect) device, the first data transfer request

corresponding to a first channel, the second data transfer request corresponding to a second channel;

initiating respective first and second delayed transactions corresponding to the first and second data transfer requests at a PCI bridge;

setting up a first pre-fetch buffer corresponding to the first delayed transaction, the first pre-fetch buffer having a first buffer fill watermark;

setting up a second pre-fetch buffer corresponding to the second delayed transaction, the second pre-fetch buffer having a second buffer fill watermark;

monitoring each of the first and second pre-fetch buffers to determine if the fill lever of a buffer meets or exceeds its buffer fill watermark, that pre-fetch buffer being a first filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the PCI bridge;

mapping a virtual buffer to the first filled buffer;

transferring data from the first filled buffer to multi-channel PCI device until the first filled buffer is empty; and

disconnecting the multi-channel PCI device from the PCI bridge.

9. The method of claim 8, further comprising:

determining that a pre-fetch buffer other than the first filled buffer has been filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the PCI bridge; and

mapping the virtual buffer to the second filled buffer;

transferring data from the second filled buffer to the multi-channel PCI device until the second filled buffer is empty; and

disconnecting the multi-channel PCI device from the PCI bridge.

10. The method of claim 8, wherein the multi-channel PCI device comprises a mass storage controller.

11. The method of claim 10, wherein the multi-channel PCI device comprises a dual-channel PCI SCSI (Small Computer System Interface) controller.

12. The method of claim 8, wherein each of the first and second data transfers comprises a transfer of data stored in memory to the multi-channel PCI device.

13. The method of claim 8, wherein the PCI bridge comprises a host-to-PCI bridge.

14. The method of claim 8, wherein the PCI bridge comprises a PCI-to-PCI bridge.

15. An apparatus, comprising:

an integrated circuit comprising circuitry to effectuate a PCI (Peripheral Component Interconnect) bridge, including:

a primary bus unit including a primary bus interface;

a secondary bus unit including a secondary bus interface; and

programmed logic to perform operations including:

receiving first and second read requests from a multi-channel PCI device coupled to the secondary bus interface, the first read request corresponding to a first channel and having an initial size, the

second read request corresponding to a second channel and having an initial size;

initiating respective first and second delayed transactions corresponding to the first and second read requests;

setting up a first pre-fetch buffer corresponding to the first delayed transaction, the first pre-fetch buffer having a first buffer fill watermark;

setting up a second pre-fetch buffer corresponding to the second delayed transaction, the second pre-fetch buffer having a second buffer fill watermark;

monitoring each of the first and second pre-fetch buffers to determine if the fill lever of a buffer meets or exceeds its buffer fill watermark, that pre-fetch buffer being a first filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the secondary bus unit; and

mapping a virtual buffer to the first filled buffer;

transferring data from the first filled buffer to the multi-channel PCI device until the first filled buffer is empty; and

disconnecting the multi-channel PCI device from the secondary bus unit.

16. The apparatus of claim 15, further comprising programmed logic to perform operations including:

determining that a pre-fetch buffer other than the first filled buffer has been filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the secondary bus unit;

mapping the virtual buffer to the second filled buffer;

transferring data from the second filled buffer to the multi-channel PCI device until the second filled buffer is empty; and

disconnecting the multi-channel PCI device from the secondary bus unit.

17. The apparatus of claim 15, further comprising programmed logic to perform operations including:

receiving a subsequent read request corresponding to the first read request;

determining whether a size of the subsequent read request is less than the first buffer fill watermark; and

in response thereto,

setting the second buffer fill watermark equal to the size of the subsequent read request.

18. The apparatus of claim 17, further comprising:

a plurality of configuration registers, each including a field to define a size of a subsequent read request buffer fill watermark

19. The apparatus of claim 15, wherein the primary bus interface comprises an interface to a host bus and the secondary bus interface comprises an interface to a PCI root bus.

20. The apparatus of claim 15, wherein each of the first and secondary bus interfaces comprises an interface to a PCI bus.

21. The apparatus of claim 15, further comprising a configuration register to store a buffer fill watermark value.

22. A computing platform, comprising:

a motherboard including a host bus and a PCI (Peripheral Component Interconnect) bus;

a processor operatively coupled to the host bus;

memory operatively coupled to the host bus; and

a host-to-PCI bridge including a primary bus unit having an interface coupled to the host bus and a secondary bus unit having an interface coupled to the PCI bus, the host-to-PCI bridge further including programmed logic to perform operations including:

receiving first and second read requests from a multi-channel PCI device coupled to the PCI bus, the first read request corresponding to a first channel and having an initial size, the second read request corresponding to a second channel and having an initial size;

initiating respective first and second delayed transactions corresponding to the first and second read requests;

setting up a first pre-fetch buffer corresponding to the first delayed transaction, the first pre-fetch buffer having a first buffer fill watermark;

setting up a second pre-fetch buffer corresponding to the second delayed transaction, the second pre-fetch buffer having a second buffer fill watermark;

monitoring each of the first and second pre-fetch buffers to determine if the fill lever of a buffer meets or exceeds its buffer fill watermark, that pre-fetch buffer being a first filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the secondary bus unit;

mapping a virtual buffer to the first filled buffer;

transferring data from the first filled buffer to the multi-channel PCI device until the first filled buffer is empty; and

disconnecting the multi-channel PCI device from the secondary bus unit.

23. The computing platform of claim 22, wherein the host-to-PCI bridge further comprises programmed logic to perform operations including:

determining that a pre-fetch buffer other than the first filled buffer has been filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second filled buffer;

and in response thereto,

connecting the multi-channel PCI device to the secondary bus unit;

mapping the virtual buffer to the second filled buffer;

transferring data from the second filled buffer to the multi-channel PCI device until the second filled buffer is empty; and

disconnecting the multi-channel PCI device from the secondary bus unit.

24. The computing platform of claim 22, wherein the host-to-PCI bridge further comprises a configuration register to store a buffer fill watermark value.

25 The computing platform of claim 22, further comprising an integrated multi-channel PCI device coupled to the PCI bus.

26. The computing platform of claim 25, wherein the integrated multi-channel PCI device comprises a dual channel SCSI (Small Computer System Interface) controller.

27. The computing platform of claim 22, wherein the host-to-PCI bridge is integrated on a platform chipset.